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(54) The use of palladium as an adhesion layer and as an electrode in ferroelectric memory devices.

(57) A ferroelectric capacitor for a ferroelectric memory device includes a substrate (10), a silicon dioxide layer (20), a palladium adhesion layer (30), a bottom electrode (40) of platinum, a metal or an alloy, a ferroelectric material (50) and a top electrode (60) of platinum, a metal or an alloy.

FIG. 1a

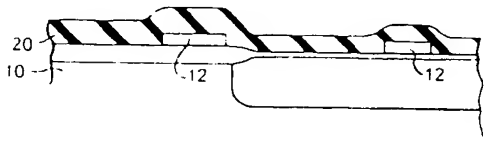


FIG. 1b

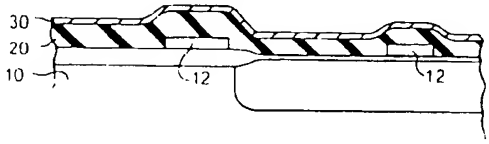


FIG. 1c

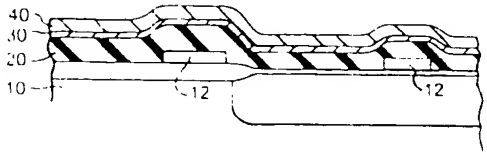
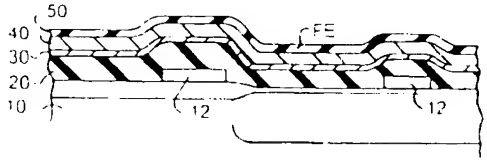


FIG. 1d



EP 0 567 878 A1

FIG. 1e

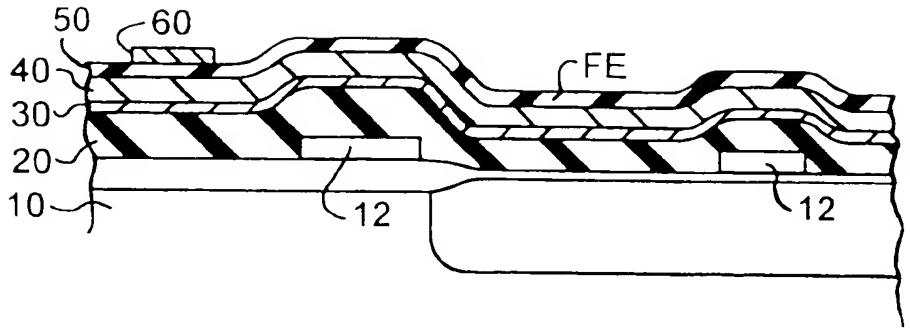
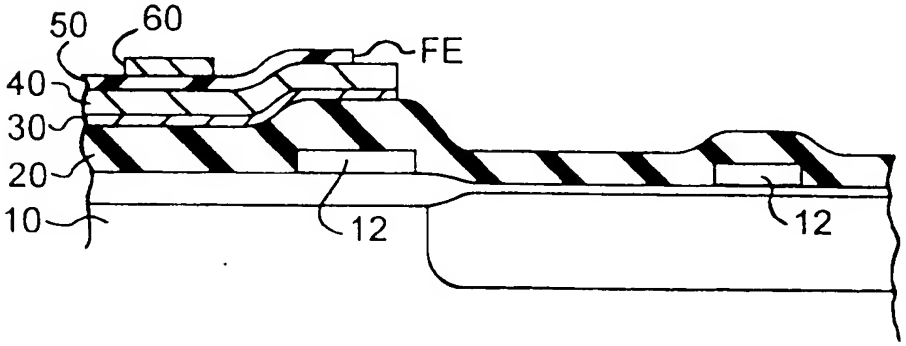


FIG. 1f



The present invention relates to the use of palladium (Pd) in ferroelectric memory devices and in particular, ferroelectric capacitors.

Ferroelectric capacitors are of interest today because of their use in ferroelectric memories and thin film discrete capacitors. See U.S. Patent Nos 4,873,664; 4,809,225; 4,853,893; 4 918,654; 4,910,708; 4,914,627; 4,893,272; 4,888,733, all issued to Ramtron Corporation of Colorado Springs, Colorado, USA.

Platinum (Pt) electrodes are often used in the fabrication of ferroelectric capacitors. Unfortunately, currently a number of problems exist with the use of these Pt electrodes in ferroelectric capacitors, not the least of which is the high cost of platinum.

Ferroelectric capacitors are fabricated using an oxide known as "PZT" which refers generally to a mixture or solution comprised of oxides of lead, zirconium and titanium, forming a .perovskite structure. The PZT is sandwiched between electrodes typically comprised of noble metals, termed lower and upper electrodes. The lower electrode may be deposited directly on silicon dioxide or some other suitable dielectric. When using Pt (or another noble metal) in the fabrication of a ferroelectric capacitor, the adhesion at the interface between the Pt or other noble metal and the dielectric is poor. If there is poor adhesion at this interface, delamination can potentially occur between the electrode and the dielectric. In addition, the adhesion of the electrode/dielectric/electrode to the substrate is also poor. The substrate typically comprises silicon covered with a layer of silicon dioxide which has a thickness in the range between 5,000 Å (500 nm) and 8,000 Å (800 nm).

Presently, one approach for solving this adhesion problem is to use titanium (Ti) or chromium (Cr) under the Pt as a "glue" layer. However, both Ti and Cr can readily diffuse through the Pt. If the Ti or Cr does diffuse through the Pt and is able to reach the PZT interface, the Ti or Cr will oxidize and will result in the degradation of the electrical properties of the capacitor.

One possible solution to the adhesion problem between the electrodes and the dielectric is disclosed in Ramtron's U.S. Patent No. 5,142,437, entitled "Conducting Electrode Layers For Ferroelectric Capacitors In Integrated Circuits And Method" which is incorporated herein by reference.

Accordingly, the main object of the present invention is to create a ferroelectric capacitor structure that overcomes the deficiencies of the prior devices.

The present invention in one of its aspects is directed to a ferroelectric capacitor for use in ferroelectric memory devices. In particular, the present invention is directed to the use of palladium or an alloy of platinum and another metal in the ferroelectric capacitor.

In a first embodiment of the present invention, an adhesion layer, comprised of palladium, is located over a silicon dioxide layer which is over a substrate A bottom electrode, a layer of ferroelectric material and a top electrode are located over the adhesion layer. The palladium adhesion layer adheres to the silicon dioxide layer while providing a good interface with the bottom electrode.

In a second embodiment, an adhesion layer is located over a substrate. A silicon dioxide layer is located between the substrate and the adhesion layer. A bottom electrode, comprising an alloy of platinum and another metal, is located over the adhesion layer. A layer of ferroelectric material and a top electrode are located over the bottom electrode. The top electrode comprises an alloy of platinum and a metal.

In a third embodiment, an adhesion layer is located over the substrate. A silicon dioxide layer is located between the substrate and the adhesion layer. A bottom electrode structure, comprising multiple layers of palladium and platinum, is located over the adhesion layer. A layer of ferroelectric material and a top electrode, comprising multiple layers of palladium and platinum, are located over the bottom electrode. The multiple layers of both the top and bottom electrode comprise two separate layers of platinum, over a layer of palladium. A further layer of palladium can be located between the two platinum layers.

In a fourth embodiment, an adhesion layer is located over the substrate. A silicon dioxide layer is located between the substrate and the-adhesion layer. A bottom electrode structure, comprising multiple layers of palladium and platinum, is located over the adhesion layer. A layer of ferroelectric material and a top electrode, comprising multiple layers of palladium and platinum, are located over the bottom electrode. The multiple layers of both the top and bottom electrode can comprise two layers of platinum separated by a layer of palladium.

The present invention is further directed to a method for forming a ferroelectric capacitor. In general, the method comprises a number of steps wherein an adhesion layer is established over a substrate, and a bottom electrode, a layer of ferroelectric material and a top electrode are established over the adhesion layer and patterned and annealed.

In describing the preferred embodiment, reference is made to the accompanying drawings wherein like parts have like reference numerals, and wherein.

FIGURE 1(a) is a cross-sectional view of a portion of a ferroelectric capacitor according to a first embodiment of the present invention showing a silicon dioxide layer over a substrate;

FIGURE 1(b) shows the structure of FIGURE 1(a) with an adhesion layer over the silicon dioxide layer.

FIGURE 1(c) shows the structure of FIGURE 1 (b) with a bottom electrode over the adhesion layer.

FIGURE 1(d) shows the structure of FIGURE 1(c) with a layer of ferroelectric material over the bottom electrode.

FIGURE 1(e) shows the structure of FIGURE 1(d) with a patterned top electrode over the layer of ferroelectric material;

FIGURE 1(f) shows that structure of Figure 1(e) after the dielectric and bottom electrode have been patterned;

FIGURE 2(a) is a cross-sectional view of a portion of a ferroelectric capacitor according to a second embodiment of the present invention showing an adhesion layer over a silicon dioxide layer over a substrate;

FIGURE 2(b) shows the structure of FIGURE 2 (a) with a bottom electrode over the adhesion layer;

FIGURE 2(c) shows the structure of FIGURE 2(b) with a layer of ferroelectric material and top electrode over the bottom electrode;

FIGURE 2(d) shows the structure of FIGURE 2(c) after the layers have been patterned;

FIGURE 3(a) is a cross-sectional view of a portion of a ferroelectric capacitor according to a third embodiment of the present invention showing a bottom electrode structure over an adhesion layer over a silicon dioxide layer over a substrate;

FIGURE 3(b) shows the structure of FIGURE 3(a) with a layer of ferroelectric material over the bottom electrode structure and a top electrode structure over the layer of ferroelectric material.

FIGURE 3(c) shows the structure of FIGURE 3(b) after the layers have been patterned;

FIGURE 4(a) is a cross-sectional view of a portion of a ferroelectric capacitor according to a fourth embodiment of the present invention showing a bottom electrode structure over an adhesion layer over a silicon dioxide layer over a substrate; and

FIGURE 4(b) shows the structure of FIGURE 4(a) with a layer of ferroelectric material over the bottom electrode structure and a top electrode structure over the layer of ferroelectric material, and

FIGURE 4(c) shows the structure of FIGURE 4(c) after the layers have been patterned.

Figures 1(a) - (e) illustrate the steps of a method for fabricating a ferroelectric capacitor having an adhesion layer comprised of palladium, according to a first embodiment of the present invention. Substrate 10 comprises the first layer of the structure. Typically, substrate 10 will be comprised of single crystal or polycrystalline silicon but could be any other common substrate such as glass, gallium arsenide, etc. Substrate 10 may include a gate electrode 12. A silicon dioxide layer 20 can then be established over substrate 10. Layer 20 can be established by wet and dry oxidation or by a variety of physical and chemical deposition techniques which are known in the art. Layer 20 typically has a thickness of 5,000 Å (500 nm) to 8,000 Å (800 nm).

Next, an adhesion layer 30 is established by sputtering or other physical deposition methods over silicon dioxide layer 20, as shown in Figure 1(b). Adhesion layer 30 typically has a thickness in the range of 100 Å (10 nm) to 200 Å (20 nm). In the preferred embodiment, adhesion layer 30 is comprised of sputtered palladium (Pd). Pd replaces titanium (Ti) which was used as the adhesion layer in the prior devices. Pd is not as reactive as Ti and minimizes the high reactivity that is observed with Ti during device processing, such as the formation of titanium oxide between the electrode and the ferroelectric material. When adhesion layer 30 is comprised of Pd, the Pd forms an oxide which adheres to the silicon dioxide. In addition, since the lattice structure of Pd matches very well with that of Pt, the interface between the Pt electrode and the adhesion layer is very good.

As shown in Figure 1(c), a bottom electrode 40 is then established over adhesion layer 30. Bottom electrode 40 is established by sputtering for example. Typically, bottom electrode 40 is comprised of a noble metal. Preferably, electrode 40 is comprised of platinum (Pt) . However, electrode 40 could also be comprised of an alloy of Pt and another metal, see infra. The thickness of electrode 40 is in the range from 1,000 Å (100 nm) to 4,000 Å (400 nm).

After layer 40 is deposited, the layer can be annealed. If annealed, a rapid thermal anneal (RTA) for no longer than 20 seconds in an inert atmosphere, such as Argon for example, is preferably used. However, it is not necessary to anneal layer 40 for the capacitor to work satisfactorily.

A dielectric 50 is then established over electrode 40, as shown in Figure 1(d). Dielectric 50 can be comprised of a ferroelectric material, such as, for example, a compound comprising lead zirconate titanate, called "PZT", and having the general formula $Pb(Ti_xZr_{1-x})O_3$. The $Pb(Ti_xZr_{1-x})O_3$ stoichiometry can be in the range from X = 1 to X = 0 1 and may include a variety of dopants. Dielectric 50 is established by sputtering for example (or sol-gel methods or a variety of other techniques), and has a thickness between 1,000 Å (100 nm) to 4,000 Å (400 nm).

After layer 50 is deposited, the structure has to be annealed in order to form the ferroelectric pervoskite phase since, in the as-deposited state the dielectric is amorphous. The annealing should be in oxygen. A RTA process can be used at a temperature between 500 °C and 850 °C for between 5 seconds and 60 seconds. A furnace could also be used at a temperature between 500 C to 750 °C for between 15 minutes and 60 minutes. Either process will produce acceptable results.

A top electrode 60 is then established over dielectric 50. Top electrode 60 can be established by sput

tering, for example Electrode 60 preferably is comprised of a noble metal, such as platinum, for example. However, other noble metals or alloys of such noble metals can be used. Electrode 60 has a thickness in the range between 1,000 Å (100 nm) to 4,000 Å (400 nm). Top electrode 60 is then patterned. Electrode 60 can be patterned by ion milling, plasma etching or wet etching, for example. The resulting cross-sectional structure is shown in Figure 1(e).

After top electrode 60 has been deposited and patterned, the whole structure should be annealed. Either RTA or furnace annealing can be used. The atmosphere needs to be oxidizing. If a RTA process is used, the temperature can be between 500°C and 850°C for between 5 seconds to 60 seconds. If a furnace anneal is used, the temperature can be between 500°C and 750°C for between 15 and 60 minutes.

Thereafter, dielectric 50 is patterned by ion milling, plasma etching or wet etching, for example. Bottom electrode 40 is then patterned in a similar manner as dielectric 50. Figure 1(f) shows the resulting structure. In a method for forming the second embodiment of the present invention, a substrate 10, a gate electrode 12 and a silicon dioxide layer 20 are formed in a manner similar to that shown in Figure 1(a) for the method for forming the first embodiment. Figures 2(a) - 2(d) show the remaining steps for the method for fabrication of the capacitor of the third embodiment.

An adhesion layer 31 is established over layer 20, as shown in Figure 2(a). Adhesion layer 31 can be comprised of, for example, Ti, as in the prior devices, or Pd, as is disclosed in the first embodiment of the present invention. Layer 31 can be established by sputtering, for example and has a thickness between 100 Å (10 nm) and 200 Å (20 nm).

A bottom electrode 40(a) is then established over layer 31, as shown in Figure 2(b). Bottom electrode 40(a) is established by sputtering, for example. Electrode 40(a) is preferably comprised of an alloy of Pt and some other metal. Electrode 40(a) can be either sputtered from a single metallic target with the desired composition or co-sputtered from two targets in the same sputtering machine. Care must be taken when co-sputtering is used to ensure that the desired composition is achieved. Electrode 40(a) can be annealed in a manner similar to that for the bottom electrode of the first embodiment. Examples of metals which can be used as alloys with Pt in electrode 40(a) include palladium (Pd), rhodium (Rh), iridium (Ir), nickel (Ni), osmium (Os), ruthenium (Ru), copper (Cu), and tungsten (W). However this is not a complete list and other metals may also be successfully utilized as alloys with Pt. In a preferred embodiment, the alloy comprises Pt and less than 10% of Pd in Pt since this composition will avoid oxidation.

By using an alloy of Pt and another metal, the amount of Pt needed in the electrode is reduced which, because of the high cost of Pt, reduces the cost of the capacitor. Further, using such an alloy will affect the electrical resistivity of the electrode. For example, the resistivity of pure Pt would be 106 nΩm at 20°C. However, an alloy of Pt and Ir (Pt-10%Ir) would increase the resistivity to 250 nΩ m at 20°C. As a result, up to 10% of Pd, Rh or Ir can be used in an alloy with Pt while still having the acceptable resistivity. The same effect can be achieved for an alloy of Pt and 4% of Os or Ni, or 2% of Ru, W or Cu.

One of the limitations, however, of using an alloy of Pt and another metal is due to the selective oxidation of the metals at high oxidizing temperatures which are often present during ferroelectric processing. For example, palladium oxide is stable between 400°C and 750°C. However, at over 750°C, it decomposes. A Pt-Rh alloy, with a Rh content below 20%, should provide better performance under oxidizing conditions. It is therefore necessary, when using an alloy of Pt and another metal, to keep annealing temperatures reasonable so as to minimize electrode degradation.

A dielectric 50, preferably comprising a layer of ferroelectric material such as that described in the first embodiment, is then established over layer 40(a). Preferably, dielectric 50 has a thickness between 1,000 Å (100 nm) and 4,000 Å (400 nm). Dielectric 50 is then annealed in a manner similar to that described for the first embodiment. A top electrode 60(a) is then established over dielectric 50, as shown in Figure 2(c). Layer 60(a) can be established by and comprise similar materials as that disclosed for layer 40(a) and has a similar thickness. However, layer 60(a) need not comprise the same materials as layer 40(a). Layers 60(a), 50 and 40(a) are patterned, and the structure is then annealed in a manner similar to that described for the first embodiment. Figure 2(d) shows the resulting structure.

In the method for forming the third embodiment of the present invention, as shown in Figure 2(a), a substrate 10, a gate electrode 12, a silicon dioxide layer 20, and an adhesion layer 31 are established, as previously described in the method for forming the second embodiment. Adhesion layer 31 is comprised of sputtered Ti with same thickness as adhesion layer 30 in the first embodiment.

A bottom electrode structure 40(b) is then formed over layer 31. Structure 40(b) is formed by initially establishing a first layer 41, comprised of Pd, over layer 31. First layer 41 is established by sputtering, for example and has a thickness between 100 Å (10 nm) and 200 Å (20 nm). A second layer 42, comprised of Pt, is then established over layer 41. Second layer 42 is established by sputtering, for example and has a thickness between 100 Å (10 nm) and 200 Å (20 nm). A third layer 43, comprised of palladium, can then be established over layer 42. Third layer 43 is optional and need not be fabricated for successful operation of

the capacitor of the present invention. Layer 43 can be established by sputtering, for example and has a thickness between 100 Å (10 nm) and 200 Å (20 nm). A fourth layer 44, comprised of Pt, is then established over layer 43 (or layer 42 if layer 43 is omitted). Layer 44 can be established by sputtering, for example and has a thickness of between 1,000 Å (100 nm) and 3,000 Å (300 nm). Figure 3(a) shows the resulting structure.

After the deposition of the bottom electrode structure, the structure may be annealed in a manner similar to that described for the bottom electrode of the first embodiment. Palladium is used in the bottom electrode structure to improve adhesion and to lower the cost of the structure. Rh, Ir, Ni, Os, Ru, Cu or W could be substituted for the Pd in the bottom electrode structure.

A layer of ferroelectric material 50 is then established over bottom electrode 40(b). Layer 50 is established and annealed in a similar manner as that disclosed in the method for forming the first embodiment.

A top electrode 60(b) is then established over layer 50. Top electrode 60(b) preferably comprises a fifth layer 61, comprised of Pd, with a thickness between 100 Å (10 nm) to 200 Å (20 nm), a sixth layer 62, comprised of Pt, with a thickness between 100 Å (10 nm) to 200 Å (20 nm) , an optional seventh layer 63 comprised of Pd with a thickness between 100 Å (10 nm) to 200 Å (20 nm) and an eighth layer 64 comprised of Pt with a thickness between 1,000 Å (100 nm) and 3,000 Å (300 nm) as shown in Fig. 3(b).

After deposition of the top electrode structure, the entire structure can be annealed and patterned as described previously for the first embodiment. Figure 3(c) shows the resulting structure. Rh, Ir, Ni, Os, Ru, Cu or W could be substituted for the Pd in the top electrode.

In this embodiment, ferroelectric material 50 is immediately sandwiched between Pt (layer 44) and Pd (layer 62) which creates asymmetric interfaces. Asymmetric ferroelectric capacitors are disclosed in Ramtron's copending U.S. Patent application serial no. 07/853,901, filed March 19, 1992 and entitled "A Method For Intercasing The Dielectric Constant Of Integrated Ferroelectric Capacitors" which is incorporated herein by reference (attorney docket no. RAM 341).

In the method for forming the fourth embodiment of the present invention, as shown in Figure 2(a), a substrate 10, a silicon dioxide layer 20 and adhesion layer 31 are formed, as previously described in the method for forming the third embodiment.

A bottom electrode structure 40(c) is then formed over layer 31. Structure 40(c) is preferably comprised of a first layer 45, comprised of Pt, having a thickness between 100 Å (10 nm) to 200 Å (20 nm) , a second layer 46, comprised of Pd, having a thickness between 100 Å (10 nm) to 200 Å (20 nm) and a third layer 47, comprised of Pt, having a thickness between 1,000 Å (100 nm) to 3,000 Å (300 nm) . The structure can then be annealed in a manner similar to that described previously for the first embodiment. Figure 4(a) shows the resulting structure.

A layer of ferroelectric material 50 is then established over bottom electrode 40(c) and annealed, in a similar manner and with similar materials as previously described for the method for forming the first embodiment.

A top electrode structure 60(c) is then established over layer 50. Top electrode 60(c) preferably comprises a fourth layer 65, comprised of Pt, with a thickness between 100 Å (10 nm) to 200 Å (20 nm), a fifth layer 66, comprised of Pd, having a thickness between 100 Å (10 nm) to 200 Å (20 nm) and a sixth layer 67, comprised of Pt, having a thickness between 1,000 Å (100 nm) to 3,000 Å (300 nm) as shown in Fig 4(b). The structure can then be annealed and patterned in a similar manner to that described supra for the first embodiment. Figure 4(c) shows the resulting structure.

This description has been offered for illustrative purposes only and is not intended to limit the invention of this application, which is defined in the claims below.

Claims

1. A capacitor characterized by a substrate (10); a silicon dioxide layer (20) located over said substrate; an adhesion layer (30), located over said silicon dioxide layer; a bottom electrode (40) located over said adhesion layer; a layer of ferroelectric material (50) located over said bottom electrode; and a top electrode (60) located over said layer of ferroelectric material.

2. A capacitor according to Claim 1 further characterized by said adhesion layer comprising palladium.

3. A capacitor according to Claim 1 further characterized by said adhesion layer comprising titanium.

4. A capacitor according to Claim 1 or 2 further characterized by said bottom electrode comprising platinum.

5. A capacitor according to Claims 1 to 3 further characterized by said bottom electrode (40a) comprising an alloy of platinum and a metal selected from the group comprising palladium, rhodium, iridium, nickel, osmium, ruthenium, copper and tungsten.

6. A capacitor according to Claims 1 to 3 further characterized by said bottom electrode (40b) comprising a first palladium layer (41), a first platinum layer (42) over said first palladium layer, and a second platinum layer (44) over said first platinum layer.

7. A capacitor according to Claim 6 further characterized by a second palladium layer (43) being located between said first platinum layer and said second platinum layer.

8. A capacitor according to Claims 1 to 3 further characterized by said bottom electrode (40c) comprising a first platinum layer (45), a first palladium layer (46) over said first platinum layer and a second platinum layer (47) over said first palladium layer.

9. A capacitor according to Claims 1 to 3 further characterized by said ferroelectric material comprising a lead zirconate titanate composition defined by the chemical composition $Pb(Ti_xZr_{1-x})O_3$ wherein X is from 1 to 0.1.

10. A capacitor according to Claim 1 or 2 further characterized by said top electrode comprising platinum.

11. A capacitor according to Claims 1 to 3 further characterized by said top electrode (60a) comprising an alloy of platinum and a metal selected from the group comprising palladium, rhodium, iridium, nickel, osmium, ruthenium, copper and tungsten.

12. A capacitor according to Claims 1 to 3 further characterized by said top electrode (60b) comprising a first palladium layer (61), a first platinum layer (62) over said first palladium layer, and a second platinum layer (64) over said first platinum layer.

13. A capacitor according to Claim 12 further characterized by a second palladium layer (63) being located between said first platinum layer and said second platinum layer.

14. A capacitor according to Claims 1 to 3 further characterized by said top electrode (60c) comprising a first platinum layer (65), a first palladium layer (66) over said first platinum layer and a second platinum layer (67) over said first palladium layer.

FIG. 1a

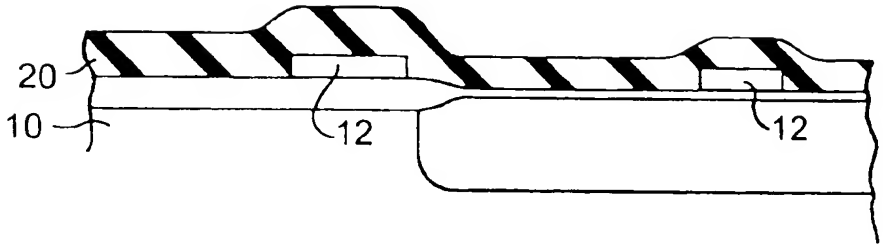


FIG. 1b

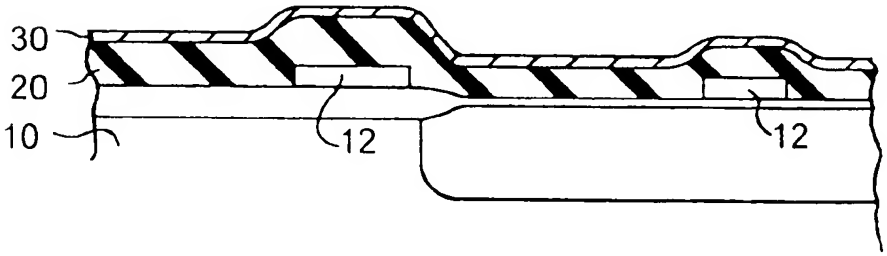


FIG. 1c

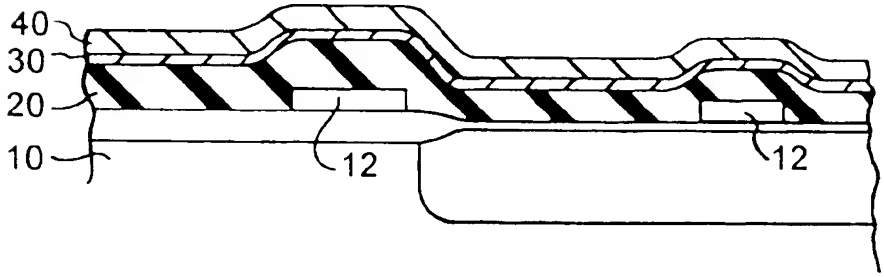


FIG. 1d

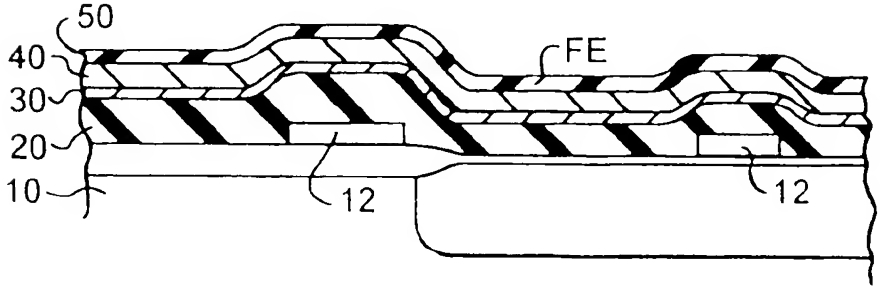


FIG. 1e

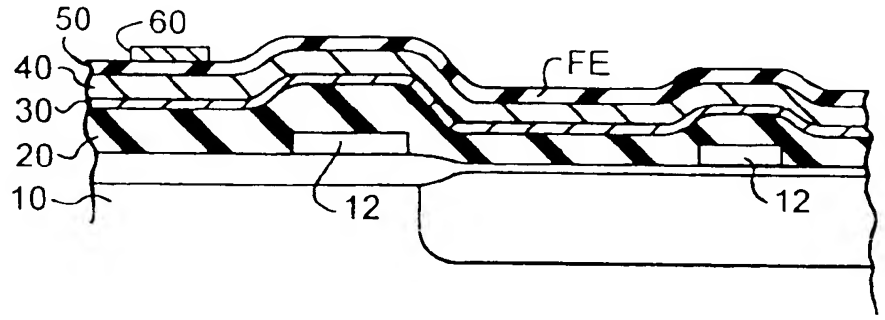


FIG. 1f

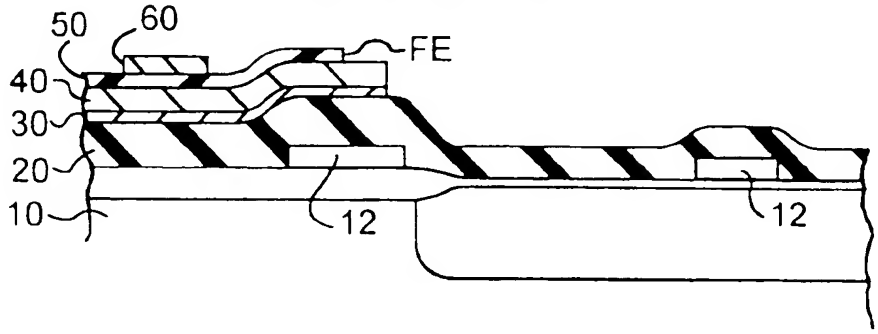


FIG. 2a

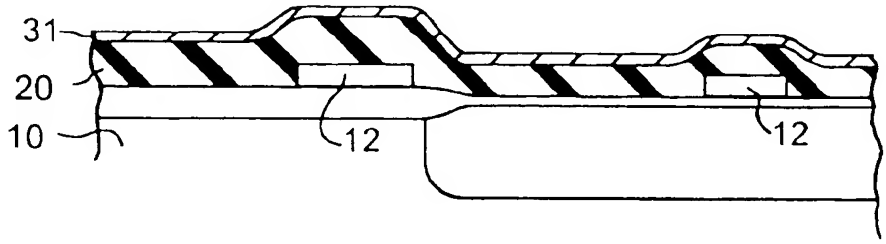


FIG. 2b

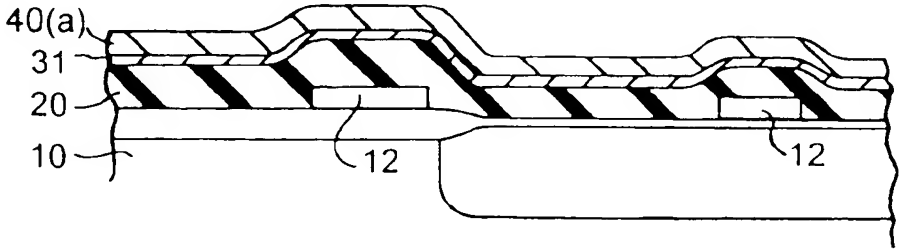


FIG. 2c

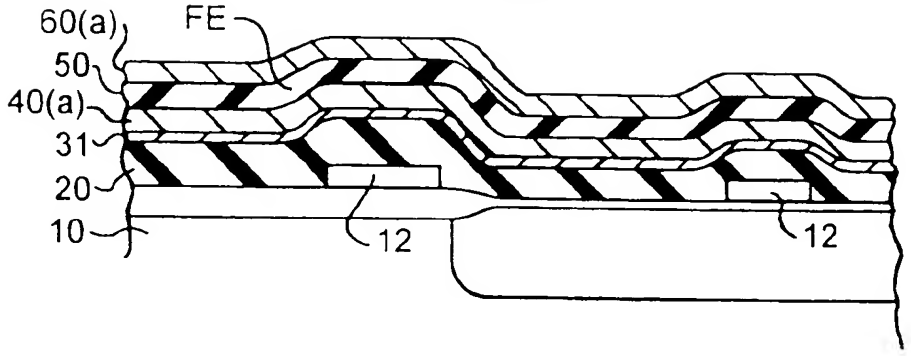


FIG. 2d

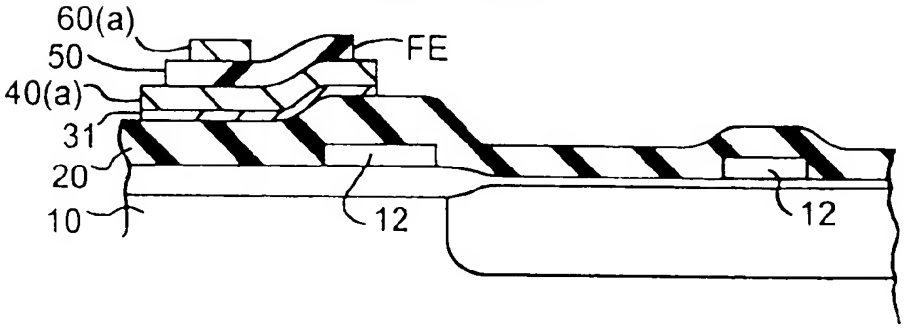


FIG. 3a

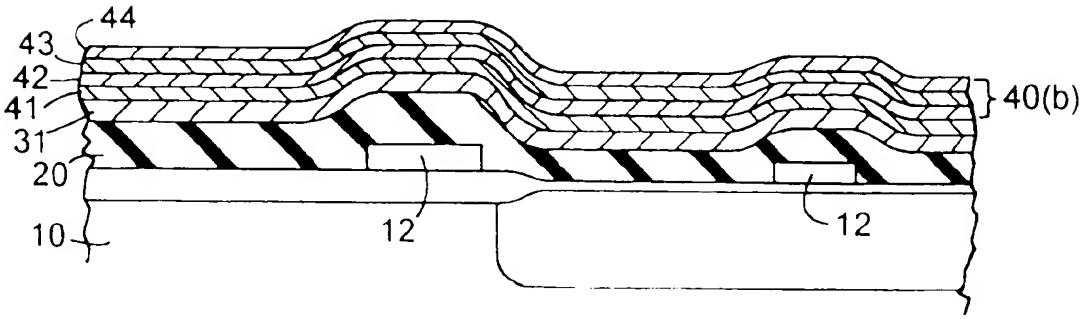


FIG. 3b

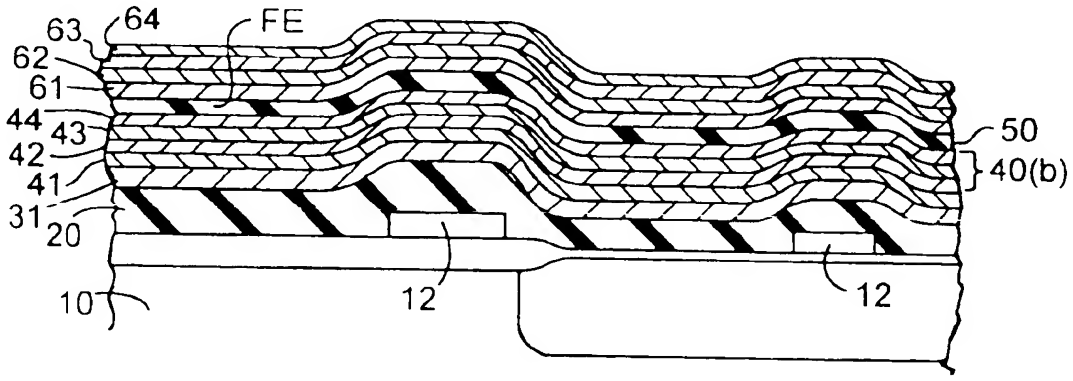


FIG. 3c

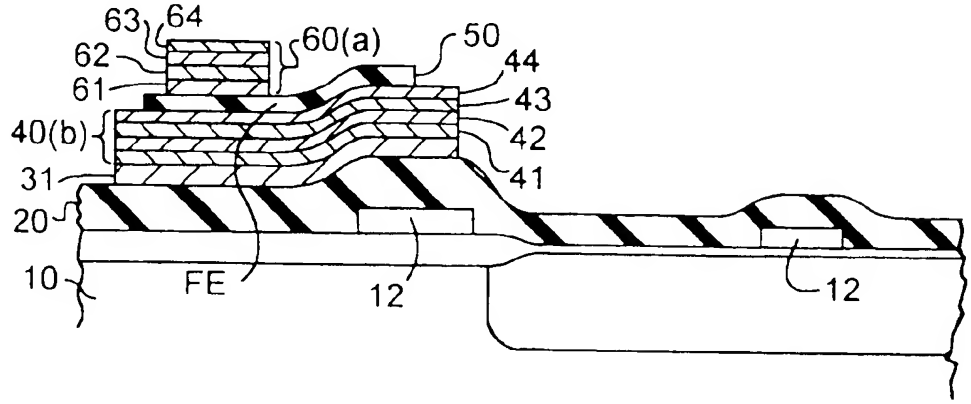


FIG. 4a

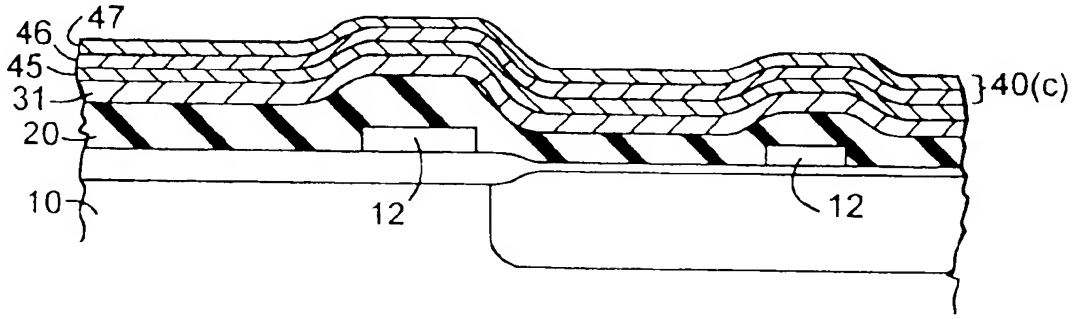
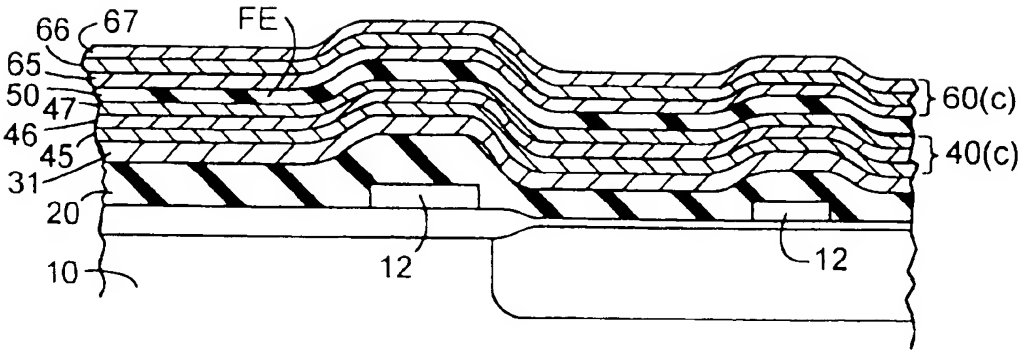


FIG. 4b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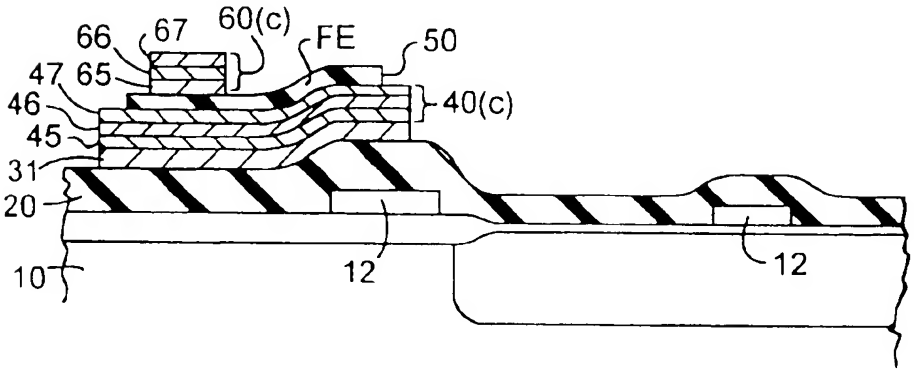
40(c)

FIG. 4c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EUROPEAN SEARCH REPORT

Application Number
EP 93 10 6289

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	JAPANESE JOURNAL OF APPLIED PHYSICS vol. 30, no. 9B, September 1991, TOKYO JP pages 2152 - 2154 KAZUHIDE ABE ET AL. 'PZT Thin Film Preparation on Pt-Ti Electrode by RF Sputtering'	1,3,4,9	H01L27/115 H01G1/01
Y	* page 2152, left column, paragraph 1 - page 2153, left column, paragraph 3; figures 2A-B *	1-2	
A	US-A-5 046 043 (NATIONAL SEMICONDUCTOR CORPORATION) 3 September 1991 * column 3, line 36 - column 4, line 32; figure 1 *	1,3,5, 10-11	
A	EP-A-0 415 751 (NEC CORP) 6 March 1991 * page 4, line 37 - page 6, line 54; claims 7,9; figure 2 *	5-9	
Y	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 28, no. 6, November 1985, NEW YORK US pages 2674 - 2675 'Unique thin film structure for high temperature substrate' * the whole article *	1-2	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H01L H01G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	05 AUGUST 1993	FRANSEN L.J.L.

CATEGORY OF CITED DOCUMENTS

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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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Docket # 2 & PTNFN 10277

Applic. # 10/027,733

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